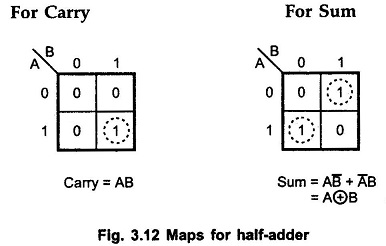
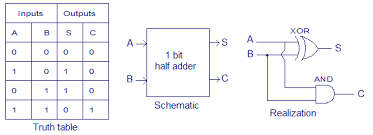
1. Implementation of half adder using gate level modeling.



**DESIGN:**

module HA(

input a,

input b,

output c\_out,

output sum);

xor x1(sum,a,b);

and A1(c\_out,a,b);

endmodule

**Testbench:**

//2Q. gate level implementation of half adder [test bench)

module tb;

reg in1,in2;

wire sum;

wire carry;

HA h1 ( .sum(sum), .b(in2),.a(in1),.c\_out(carry));

initial begin

$monitor (" %b + %b = %b =%d",in1,in2,{carry,sum},{carry,sum});

{in1,in2}=2'b00; #10;

{in1,in2}=2'b01; #10;

{in1,in2}=2'b10; #10;

{in1,in2}=2'b11; #10;

end

endmodule

**run.do**

# cd {C:\Users\alisy\Documents\verilog\class1\Q02\_half adder}

#environment creation

vlib work

#compilation

vlog HA\_G.v

vlog HA\_G\_tb.v

#simulation

vsim work.tb

run -all